CLOCK GENERATION CIRCUIT AND WIRELESS RECEIVING DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-180086; filed September 11, 2015; the entire contents of which are incorporated herein by reference.

FIELD

An embodiment described herein relates generally to a clock generation circuit and a wireless receiving device.

BACKGROUND

In a wireless receiving device which includes an analog circuit and a digital circuit, harmonics of a clock signal of the digital circuit are introduced into the analog circuit as unnecessary radiation (spurious), and thereby receiving sensitivity is degraded. For this reason, it is preferable that a clock signal to be supplied to a digital circuit is appropriately generated.

An example of related art includes Japanese Patent No. 4982239.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram illustrating a configuration of a clock generation circuit according to an embodiment.

FIGS. 2A to 2D are diagrams illustrating configurations of variable delay units according to the embodiment.

FIG. 3 is a diagram illustrating a configuration of a random number generation unit according to the embodiment.

FIG. 4 is a diagram illustrating a configuration of a filter according to the embodiment.

FIG. 5 is a diagram illustrating a probability distribution of random numbers according to the embodiment.

FIG. 6 is a diagram illustrating an operation of the clock generation circuit according to the embodiment.

FIG. 7 is a diagram illustrating a configuration of a wireless receiving device to which the clock generation circuit according to the embodiment is applied.

FIGS. 8A and 8B are diagrams illustrating operations of the wireless receiving device to which the clock generation circuit according to the embodiment is applied.

FIG. 9 is a diagram illustrating a configuration of a filter according to a modification example of the present embodiment.

DETAILED DESCRIPTION

[0004]An embodiment is to provide a clock generation circuit and a wireless receiving device which can appropriately generate a clock signal to be supplied to a digital circuit.

[0005]In general, according to one embodiment, a clock generation circuit including a random number generation unit, a filter, and a variable delay unit is provided. The random generation unit generates a random number having a first probability distribution. The filter changes a probability distribution of the generated random number into a second probability distribution from a first probability distribution. The variable delay unit generates a modulated clock signal by providing the amount of delay that is changed in accordance with a random number having the second probability distribution, to a clock signal which is input.

[0007]Hereinafter, a clock generation circuit according to the embodiment will be described with reference to the drawings. The exemplary embodiment is not limited to the embodiment.

Embodiment

[0008]A clock generation circuit 1 according to the embodiment is applied to, for example, a wireless receiving device. The wireless receiving device according to wireless standards such as, M-WiMAX, or WLAN and LTE requires high receiving sensitivity in order to secure a wide communication area. In the wireless receiving device, signal processing of a reception signal received in an analog manner is performed in an analog manner by an analog circuit, and signal processing of the signal in which signal processing is performed in an analog manner is performed in a digital manner by a digital circuit. In addition, miniaturization of the wireless receiving device is required, and requirements for one chip LSI of the wireless receiving device in which an analog circuit and a digital circuit are embedded together increase. In the one chip LSI, spurious due to integer harmonics of a clock signal generated by the digital circuit is leaked into an analog circuit, and thereby reception characteristics can be decreased. For this reason, countermeasures for preventing spurious from being generated in an analog circuit can be provided.

[0009]For example, in the wireless receiving device, a digital circuit performs processing of a signal in a digital manner in synchronization with a clock signal generated by the clock generation circuit 1. At this time, if the clock generation circuit 1 performs modulation by which edge timing of a clock signal to be generated is randomly changed by delaying an input clock signal using random numbers, spurious can be diffused in a power manner on a frequency spectrum.

[0010]However, the spurious can remain at a predetermined frequency without being diffused. For example, if a phase difference corresponding to the amount of shift of edge timing of a clock pulse of a reference clock signal is randomly changed in a range of 0° to 360° with respect to one period of a spurious frequency, amplitude of a maximum phase difference (360°) amplitude of a minimum phase difference (0°) in the range overlap each other, when viewed from a phase difference and an amplitude plane (complex plane), and thus the spurious is hardly diffused electrically. For this reason, the spurious easily remains at a frequency corresponding to a maximum phase difference.

[0011]Hence, in the embodiment, remaining of spurious is reduced by changing a probability distribution of random numbers which are used for modulation in which edge timing is changed by the clock generation circuit 1 such that probabilities of a minimum value and a maximum value are reduced more than probability of a median value.

[0012]Specifically, as illustrated in FIG. 1, the clock generation circuit 1 receives an input clock signal fCKin through an input terminal 2, and generates an output clock signal (modulated clock signal) fCKout by providing the amount of delay changed in accordance with random numbers to the input clock signal fCKin. At this time, the random numbers has a probability distribution which is changed such that probabilities of a minimum value and a maximum value are reduced more than probability of a median value. The clock generation circuit 1 outputs the generated output clock signal fCKout from an output terminal 3. FIG. 1 is a diagram illustrating a configuration of the clock generation circuit 1.

[0013]The clock generation circuit 1 includes a random number generation unit 10, a filter 20, and a variable delay unit 30. The random number generation unit 10 and the filter 20 are connected in parallel with a signal line 4 which connects the input terminal 2 to the variable delay unit 30, between the input terminal 2 and the variable delay unit 30.

[0014]The variable delay unit 30 receives random numbers from the filter 20 and receives the input clock signal fCKin through the signal line 4 from the input terminal 2. The variable delay unit 30 generates the output clock signal fCKout by providing the amount of delay according to random numbers to the input clock signal fCKin.

[0015]For example, as illustrated in FIG. 2A, the variable delay unit 30 may have a configuration in which the amount of delay is varied by a variable RC circuit in accordance with random numbers. FIG. 2A is a circuit diagram illustrating a configuration of the variable delay unit 30. The variable delay unit 30 illustrated in FIG. 2A includes inverters INV-1 and INV-2, a variable resistor element R, and a variable capacitor element C. The inverter INV-1 includes an input side connected to one terminal 30a of the variable delay unit 30, and an output side connected to one terminal of the variable resistor element R. The variable resistor element R includes the other terminal connected to both one terminal of the variable capacitor element C and an input side of the inverter INV-2. The variable capacitor element C includes the other terminal connected to a ground potential. The inverter INV-2 includes an output terminal connected to the other terminal 30b of the variable delay unit 30. The variable resistor element R changes a resistance value thereof into a resistance value according to random numbers which are supplied. The variable capacitor element C changes a capacitance value thereof into a capacitance value according to random numbers which are supplied. As a result, a time constant of the variable delay unit 30 is changed in accordance with random numbers, and thus the variable delay unit 30 changes the amount of delay thereof into the amount of delay according to random numbers which are supplied.

[0016]Alternatively, as illustrated in FIG. 2B, the variable delay unit 30 may have a configuration in which the amount of delay is changed by variable resistors on a power supply side and a ground side of inverters of n stages (n is even numbers greater than 2). FIG. 2B is a circuit diagram illustrating a configuration of the variable delay unit 30. The variable delay unit 30 illustrated in FIG. 2B includes n inverters INV-1 to INV-n, a variable resistor element R-2 on the power supply side, and a variable resistor element R-1 on the ground side. An inverter INV-1 of a first stage includes an input side connected the one terminal 30a of the variable delay unit 30, and an output side connected to an input side of an inverter INV-2 of the second stage. The inverter INV-2 of a second stage includes an output side connected to an input side of an inverter INV-3 of a third stage. An inverter INV-(n-1) of an (n-1)th stage includes an output side connected to an input side of an inverter INV-n of an nth stage. The inverter INV-n of the nth stage includes an output side connected to the other terminal 30b of the variable delay unit 30. The variable resistor element R-2 includes one terminal connected to a terminal on a power supply side of the n inverters INV-1 to INV-n, and the other terminal connected to a power supply potential. The variable resistor element R-1 includes one terminal connected to a terminal on a ground side of the n inverters INV-1 to INV-n, and the other terminal connected to a ground potential. The variable resistor element R-2 changes a resistance value thereof into a resistance value according to random numbers which are supplied. The variable resistor element R-1 changes a resistance value thereof into a resistance value according to random numbers which are supplied. As a result, a response speed on the power supply side and the ground side of the n inverters INV-1 to INV-n is changed in accordance with random numbers, and thus the variable delay unit 30 changes the amount of delay thereof into the amount of delay according to random numbers which are supplied.

[0017]Alternatively, as illustrated in FIG. 2C, the variable delay unit 30 may have a configuration in which the amount of delay is varied by switching a delay lien that is selected from multiple delay lines. FIG. 2C is a circuit diagram illustrating a configuration of the variable delay unit 30. The variable delay unit 30 illustrated in FIG. 2C includes multiple delay lines DL-1 to DL-n and switching circuits SW-1 and SW-2. The multiple delay lines DL-1 to DL-n respectively include inverters INV in which stages thereof are different from each other, and can provide the amounts of delay different from each other. The delay lines DL-1 includes the inverter INV-1 of one stage, and can provide the amount of delay of the amount of one stage. The delay lines DL-n includes inverters INV-1 to INV-n of n stages, and can provide the amount of delay of the amount of n stages. The switching circuit SW-1 includes multiple switches which are switched on exclusively, and switches a delay line which is connected to the one terminal 30a among the multiple delay lines DL-1 to DL-n in accordance with a switch that is switched on among the multiple switches. The switching circuit SW-2 includes multiple switches which are switched on exclusively, and switches a delay line which is connected to the other terminal 30b among the multiple delay lines DL-1 to DL-n in accordance with a switch that is switched on among the multiple switches. The switching circuit SW-1 changes a switch which is switched on into a switch according to the random numbers which are supplied. The switching circuit SW-2 changes a switch which is switched on into a switch according to the random numbers which are supplied. As a result, a delay line which is selected from the multiple delay lines DL-1 to DL-n is changed in accordance with random numbers, the variable delay unit 30 changes the amount of delay thereof into the amount of delay according to the random numbers which are supplied.

[0018]Alternatively, as illustrated in FIG. 2D, the variable delay unit 30 may have a configuration in which the amount of delay is varied by varying stages of inverters for passing through. FIG. 2D is a circuit diagram illustrating a configuration of the variable delay unit 30. The variable delay unit 30 illustrated in FIG. 2D includes n inverters INV-1 to INV-n, and a switching circuit SW-3. The switching circuit SW-3 includes multiple switches which are switched on exclusively, and switches the number of stages of inverters for passing through between the one terminal 30a and the other terminal 30b in accordance with a switch which is switched on among the multiple switches. The switching circuit SW-3 changes a switch which is switched on into a switch according to the random numbers which are supplied. As a result, the number of stages of inverters for passing through between the one terminal 30a and the other terminal 30b is varied in accordance with a time constant, and thus the variable delay unit 30 changes the amount of delay thereof into the amount of delay according to the random numbers which are supplied.

[0019]Returning to FIG. 1, the random number generation unit 10 generates random numbers having a first probability distribution. In the first probability distribution, each value of the random numbers which are generated has approximately equivalent probability. For example, as illustrated in FIG. 5, if random numbers of 0 to 15 are generated, the random number generation unit 10 generates the random numbers of 0 to 15 in approximately equivalent probability. FIG. 5 is a diagram illustrating a probability distribution of random numbers, a vertical axis denotes values of relative probability if occurrence probability in the random number generation unit 10 is set to 1, and a horizontal axis denotes values of random numbers.

[0020]For example, the random number generation unit 10 can generate a random number of three bits rnd3<2:0>, using the configuration illustrated in FIG. 3. FIG. 3 is a diagram illustrating a configuration of the random number generation unit 10. The random number generation unit 10 includes a starter 11, a shift register 12, and a logic circuit 13. The starter 11 is provided so as to prevent the random number from being fixed to zero. The starter 11 includes a NOR gate 11a and an OR gate 12a. The NOR gate 11a calculates a negative logical sum of the random number rnd<0> to rnd<8>. The OR gate 12a calculates a logical sum of an output (ransom number rnd<0>) of a final stage of the shift register 12 and an output of the NOR gate 11a.

[0021]The shift register 12 includes flip-flops of nine stages FF-1 to FF-9 and the OR gate 12a. The OR gate 12a calculates a logical calculation of an output (random number rnd<5>) of the flip-flop FF-4 of a fourth stage and an output (random number rnd<0>) of the flip-flop FF-9 of a final stage, and inputs the calculated value to the flip-flop FF-5 of a fifth stage. The shift register 12 shifts bit values which are output from the OR gate 12a in synchronization with a clock signal CLK. According to this, the random numbers rnd which are output from the flip-flops FF-1 to FF-9 of each stage are changed.

[0022]The logic circuit 13 receives random numbers rnd<6>, rnd<4>, rnd<2>, and rnd<0> which are output from the flip-flops of the third, fifth, seventh, and ninth stages FF-3, FF-5, FF-7, and FF-9. The logic circuit 13 includes an inverter 13a and OR gates 13b and 13c. The inverter 13a generates a random number rnd3<0> by logically inverting the random number rnd<0>. The OR gate 13b generates a random number rnd3<1> by calculating a logical sum of the random number rnd<2> and the random number rnd<4>. The OR gate 13c generates a random number rnd3<2> by calculating a logical sum of the random number rnd<4> and the random number rnd<6>. The logic circuit 13 outputs the random number rnd3<2:0> of three bits which are generated to the filter 20.

[0023]Returning to FIG. 1, the filter 20 receives random numbers from the random number generation unit 10. The random numbers have first probability distribution. In the first probability distribution, each value of the random numbers which are generated has approximately equivalent probability. The filter 20 changes the probability distribution of the random numbers from the first probability distribution to second probability distribution. Probability of a minimum value of the random numbers in the second probability distribution is less than probability of a minimum value of the random numbers in the first probability distribution. Probability of a maximum value of the random numbers in the second probability distribution is less than probability of a minimum value of the random numbers in the first probability distribution. Probability of a median value of the random numbers in the second probability distribution is more than probability of a median value of the random numbers in the first probability distribution.

[0024]For example, as illustrated in FIG. 5, if probability of the random numbers (random numbers of three bits) of 0 to 15 which are generated by the random number generation unit 10 is set to 1, the filter 20 sets the random numbers of 0 to 2, and 12 to 15 to probability less than 1, and sets the random numbers of 4 to 10 to probability greater than 1. The filter 20 sets probability of a minimum value 0 of the random numbers and probability of a minimum value 15 of the random numbers, to an extremely small value, and sets probability of a median value 7 of the random numbers to an extremely large value 2. The filter 20 changes a probability distribution (first probability distribution) of the random numbers into a probability distribution (second probability distribution) of a mountain type.

[0025]For example, as illustrated in FIG. 4, the filter 20 can generate the random numbers rnd4(3:0> of four bits by a configuration in which the current random number (three bits) is added to a random number (three bits) before one clock pulse. The filter 20 includes a delay unit 21 and a full addition unit 22. The delay unit 21 includes multiple flip-flops FF-11 to FF-13. The multiple flip-flops FF-11 generates the random number rnd3s<0> by delaying the random number rnd3<0> received from the random number generation unit 10 by the amount of one clock pulse, and outputs the random number rnd3s<0> to the full addition unit 22. The multiple flip-flops FF-12 generates the random number rnd3s<1> by delaying the random number rnd3<1> received from the random number generation unit 10 by the amount of one clock pulse, and outputs the random number rnd3s<1> to the full addition unit 22. The multiple flip-flops FF-13 generates the random number rnd3s<2> by delaying the random number rnd3<2> received from the random number generation unit 10 by the amount of one clock pulse, and outputs the random number rnd3s<2> to the full addition unit 22.

[0026]The full addition unit 22 adds the random number rnd3<2:0> of three bits received from the random number generation unit 10 to the random number rnd3s<2:0> of three bits received from the delay unit 21, and outputs the addition results to the variable delay unit 30 as the random number rnd4<3:0> of four bits.

[0027]For example, if the probability distribution (first probability distribution) represented by “random number” illustrated in FIG. 5 is changed into a probability distribution (second probability distribution) represented by “random number+filter”, and the variable delay unit 30 is operated by the random number having the second probability distribution, remaining of the spurious can be reduced, as illustrated in FIG. 6. FIG. 6 is a diagram illustrating an operation of the clock generation circuit 1.

[0028]That is, if a horizontal axis denotes a maximum value (maximum phase difference) of a range in which a phase difference corresponding to the amount of shift of edge timing of a clock signal is varied in order to diffuse the spurious on a frequency spectrum in a power manner, and a vertical axis denotes the amount of remaining spurious (power level), the characteristics illustrated in FIG. 6 are obtained. A phase difference corresponding to the amount of shift of edge timing of a clock signal is represented by a unit of a phase (phase angle) with respect to one period of a spurious frequency. If characteristics represented by “random number” is compared with characteristics represented by “random number+filter”, it is possible to confirm that the remaining spurious is reduced near, for example, 720°. That is, it can be seen that the effect of overlapping of amplitude of a maximum phase difference (720°) and amplitude of a minimum phase difference (0°) can be effectively reduced by an action of the filter 20, if a phase difference between rising edge timing and falling edge timing of a clock pulse is randomly changed in a range of 0° to 720°.

[0029]Subsequently, a wireless receiving device 100 to which the clock generation circuit 1 is applied will be described with reference to FIG. 7. FIG. 7 is a diagram illustrating a configuration of the wireless receiving device 100.

[0030]The wireless receiving device 100 includes an antenna AT, an analog circuit 160, a digital circuit 170, an original oscillator XO, a local oscillation circuit SYN, and clock generation circuits 1-1 and 1-2. The analog circuit 160 includes a low noise antenna LNA, a mixer MIX, a low pass filter LOW PASS FILTER, and a variable amplifier AMP. The digital circuit 170 includes an AD converter ADC and a digital processing circuit DPC. In the wireless receiving device 100, the clock generation circuits 1-1 and 1-2 are respectively provided with respect to the AD converter ADC and the digital processing circuit DPC, and are configured such that operations of modulating the clock signal can be on/off separately from each other.

[0031]In the wireless receiving device 100, if clock modulation operations of the clock generation circuits 1-1 and 1-2 are off, spurious components denoted by arrows of FIG. 8A can be generated. In contrast to this, if clock modulation operations are on, spurious components denoted by arrows of FIG. 8B can be generated. FIG.s 8A and 8B are respectively diagram illustrating an operation of the wireless receiving device 100, a vertical axis denotes power, and a horizontal axis denotes a frequency. When the clock modulation operation is on (FIG. 8B), unnecessary spurious components are newly generated in a frequency which is not generated when the clock modulation operation is off (FIG. 8A). For this reason, a function of making the clock modulation operations of the clock generation circuits 1-1 and 1-2 on/off is effective according to the frequency bands to be used.

[0032]For example, if a receiving channel is a signal denoted by a one-dotted chain line of FIG. 8A, a frequency with the spurious components denoted by arrows does not overlap a frequency of a desired signal. For this reason, the digital processing circuit DPC controls the clock generation circuits 1-1 and 1-2 such that the clock modulations performed by the clock generation circuits 1-1 and 1-2 are off. The clock generation circuits 1-1 and 1-2 continuously output the reference clock signal (output clock signal fCKout which provides a constant amount of delay to the input clock signal fCKin). Meanwhile, if a receiving channel is a signal denoted by a dashed line of FIG. 8B, the frequency with the spurious components denoted by the arrows overlaps a frequency of a desired signal. For this reason, the digital processing circuit DPC controls the clock generation circuits 1-1 and 1-2 such that the clock modulations performed by the clock generation circuits 1-1 and 1-2 are on. The clock generation circuits 1-1 and 1-2 output clock signals obtained by modulating edge timing by the amount of delay according to the random numbers with respect to the input clock signal. In FIGS. 8A and 8B, vertical axes denote a power level, and a horizontal axes denote a frequency, respectively.

[0033]Alternatively, for example, if a signal level is high and the effect of spurious on a receiving signal decreases, necessity for modulating the clock signal decreases. For this reason, the digital processing circuit DPC controls the clock generation circuits 1-1 and 1-2 such that the clock modulations performed by the clock generation circuits 1-1 and 1-2 are off. The clock generation circuits 1-1 and 1-2 continuously output the reference clock signal. Meanwhile, if a signal level is low and the effect of spurious on a receiving signal decreases, necessity for modulating the clock signal increases. For this reason, the digital processing circuit DPC controls the clock generation circuits 1-1 and 1-2 such that the clock modulations performed by the clock generation circuits 1-1 and 1-2 are on. The clock generation circuits 1-1 and 1-2 output clock signals obtained by modulating thereference clock signal by the amount of delay according to the random numbers.

[0034]As described above, in the embodiment, the probability distribution of the random numbers which are used for modulation in which edge timing is changed by the clock generation circuit 1 is changed so as to be less than probability of a median value. Hence, the output clock signal (modulated clock signal) is generated by providing the amount of delay which is changed in accordance with random numbers having the probability distribution to the input clock signal. As a result, the clock generation circuit 1 can reduce remaining of the spurious.

[0035]As illustrated in FIG. 9, a filter 20i may generate the random number rnd4<3:0> of four bits, using a configuration in which a random number (three bits) before one clock pulse is subtracted from a current random number (three bits). That is, the filter 20i further include an inversion circuit 23i in the configuration illustrated in FIG. 4. The inversion circuit 23i generates a random number rnd3x<2:0> which is obtained by logically inverting a random number rnd3<2:0> received from the random number generation unit 10, and outputs the random number to the full addition unit 22. The full addition unit 22 add the random number rnd3s<0> to the random number rnd3x<2:0>, and equivalently, subtracts the random number rnd3x<2:0> from the random number rnd3s<0>. As a result, in the same manner as in the embodiment, it is possible to change probability distribution of random numbers into the second probability distribution from the first probability distribution. In addition, since frequency components can be reduced, compared to the configuration illustrated in FIG. 4, the spurious is easily diffused on a frequency spectrum in a power manner.

[0036]While a certain embodiment has been described, the embodiment has been presented by way of an example only, and is not intended to limit the scope of the inventions. Indeed, the novel embodiment described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A clock generation circuit comprising:

a random generation unit which generates a random number having a first probability distribution;

a filter which changes a probability distribution of the generated random number into a second probability distribution from a first probability distribution; and

a variable delay unit which generates a modulated clock signal by providing the amount of delay that is changed in accordance with a random number having the second probability distribution, to a clock signal which is input.

2. The circuit according to Claim 1,

wherein probability of a minimum value of random numbers having the second probability distribution is less than probability of a minimum value of random numbers having the first probability distribution, and

wherein probability of a maximum value of the random numbers having the second probability distribution is less than probability of a maximum value of the random numbers having the first probability distribution.

3. The circuit according to Claim 1 or 2, wherein probability of a median value of random numbers having the second probability distribution is less than probability of a median value of random numbers having the first probability distribution.

4. The circuit according to any one of Claims 1 to 3, wherein the filter is a digital filter.

5. A wireless receiving device comprising:

the clock generation circuit described in any one of Claims 1 to 4; and

a digital circuit which receives a modulated clock signal that is generated by the clock generation circuit.

ABSTRACT

According to one embodiment, a clock generation circuit including a random number generation unit, a filter, and a variable delay unit is provided. The random generation unit generates a random number having a first probability distribution. The filter changes a probability distribution of the generated random number into a second probability distribution from a first probability distribution. The variable delay unit generates a modulated clock signal by providing the amount of delay that is changed in accordance with a random number having the second probability distribution, to a clock signal which is input.

Drawings

FIG. 4

FROM RANDOM NUMBER GENERATION UNIT 10

TO VARIABLE DELAY UNIT 30

FIG. 5

PROBABILITY (RELATIVE VALUE)

VALUE OF RANDOM NUMBER

-¨- RANDOM NUMBER

-- RANDOM NUMBER+FILTER

FIG. 6

MUCH¬REMAINING SPURIOUS®SMALL

MAXIMUM PHASE DIFFERENCE [deg]

-¨- RANDOM NUMBER

-- RANDOM NUMBER+FILTER

FIG. 7

160: ANALOG CIRCUIT

170: DIGITAL CIRCUIT

FIG. 9

FROM RANDOM NUMBER GENERATION UNIT 10